## CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. An interleaved generalized convolutional encoder, comprising:

(a) a node, the node being capable of receiving a data input, the data input being a portion of a data symbol;

(b) a memory element, the memory element being capable of storing a plurality of prior data inputs, the prior data inputs being a portion of each of a plurality of prior data symbols, the plurality of prior data inputs being subjected to a variable time delay; and

(c) a plurality of logic calculators,

(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,

(ii) the plurality of logic calculators including one or more final logic calculators, the one or more final logic calculators being capable of generating an output,

(A) the output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators, the coefficient input, and the variable time delay.

2. The encoder of claim 1, wherein the data input is a portion of a PAM symbol.

3. The encoder of claim 1, wherein the data input is processed by a serial to parallel converter prior to entering the encoder.

4. The encoder of claim 1, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

5. The encoder of claim 1, wherein the variable time delay is a plurality of unit time delays.

6. The encoder of claim 1, wherein a receiver sets the variable time delay.

7. The encoder of claim 1, wherein a receiver dynamically sets the variable time delay.

8. The encoder of claim 7, wherein the variable time delay is based on the quality of a transmission path between a transmitter and the receiver.

9. The encoder of claim 7, wherein the variable time delay is based on noise affecting the transmission of data between a DTE and the receiver.

10. The encoder of claim 1, wherein the variable time delay is three bauds.

11. The encoder of claim 1, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

12. The encoder of claim 1, wherein the output is processed by a mapper after exiting the encoder.

13. The encoder of claim 1, wherein the plurality of logic gates are implemented with firmware.

14. The encoder of claim 1, wherein the encoder is implemented with software that is executed with a processor.

15. The encoder of claim 1, wherein the variable time delay is implemented by a reference code of A=212124 octal and B=1202401 octal.

16. An interleaved generalized convolutional encoder, comprising:

(a) a variable time delay element;

(b) a switch;

(c) a plurality of convolutional encoders being capable of receiving a data input, the data input being a portion of a data symbol, wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the variable time delay element;

(d) the plurality of convolutional encoders being capable of storing a plurality of prior data inputs, the prior data inputs for any one of the convolutional encoders being a portion of each of a plurality of prior data symbols directed to the one of the convolutional encoders, the plurality of prior data inputs being subjected to a unit time delay; and

(e) a plurality of logic calculators associated with each of the plurality of convolutional encoders,

(i) a portion of the plurality of logic calculators being capable of receiving a coefficient input,

(ii) the plurality of logic calculators including at least one final logic calculator, the at least one final logic calculator being capable of producing an output,

(A) the output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators, the coefficient input, and the variable time delay element.

17. The encoder of claim 16, wherein the data input is a portion of a PAM symbol.

18. The encoder of claim 16, wherein the data input is processed by a serial to parallel converter prior to entering the switch.

19. The encoder of claim 16, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

20. The encoder of claim 16, wherein a receiver sets the delay associated with the variable time delay element.

21. The encoder of claim 16, wherein a receiver dynamically sets the delay associated with the variable time delay element.

22. The encoder of claim 21, wherein the delay associated with the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver.

23. The encoder of claim 21, wherein the delay associated with the variable time delay element is based on noise affecting the transmission of data between a DTE and the receiver.

24. The encoder of claim 16, wherein the delay associated with the variable time delay is three bauds.

25. The encoder of claim 16, wherein the plurality of logic calculators includes a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

26. The encoder of claim 16, wherein the output is processed by a mapper after exiting the encoder.

27. The encoder of claim 16, wherein the plurality of logic gates are implemented with firmware.

28. The encoder of claim 16, wherein the encoding system is implemented with software that is executed with a processor.

29. A method of converting a non-interleaving convolutional encoder defined by a reference code of ten or fewer coefficients into an interleaving generalized convolutional encoder, comprising inserting a zero coefficient between the coefficients defining the non-interleaving convolutional encoder.

30. The method of claim 29, wherein the reference code of A=212124 octal and B=1202401 octal is used to define the interleaving generalized convolutional encoder.

31. A system for encoding information, comprising:

(a) first means for receiving a data input, the data input being a portion of a data symbol;

(b) second means for variably delaying a plurality of prior data inputs, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

(c) third means for storing the variably delayed plurality of inputs;

(d) fourth means for performing logic calculations;

(e) fifth means for receiving a receiver input; and

(f) sixth means for producing an output, wherein the output is based on the operation of the first means, the second means, the third means, the fourth means, and the fifth means.

32. The system of claim 31, wherein the data input is a portion of a PAM symbol.

33. The system of claim 31, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

34. The system of claim 31, wherein a receiver determines the value of the variable delay of the means for variably delaying a plurality of inputs.

35. The system of claim 31, wherein a receiver dynamically determines the value of the variable delay of the means for variably delaying a plurality of inputs.

36. The system of claim 35, wherein a value of the variable delay is based on the quality of a transmission path between a transmitter and the receiver.

37. The system of claim 35, wherein a value of the variable delay is based on noise affecting the transmission of data between a DTE and the receiver.

38. The system of claim 31, wherein a value of the variable delay is three bauds.

39. A method for interleaving and convolutionally encoding data, the method comprising:

(a) receiving a data input, the data input being a portion of a data symbol;

(b) storing a plurality of prior data inputs, the prior data inputs being a portion of each of a plurality of prior data symbols;

(c) variably delaying the stored plurality of data inputs;

(d) receiving a coefficient input from a receiver;

(e) performing logic calculations on the received data input, the variably delayed and stored plurality of data inputs, and the coefficient input; and

(f) producing an output based on the performance of the logic calculations.

40. The method of claim 39, wherein the data input is a portion of a PAM symbol.

41. The method of claim 39, wherein the data input is received from a serial to parallel converter.

42. The method of claim 39, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

43. The method of claim 39, wherein the amount of variable delaying is dynamically determined by a receiver.

44. The method of claim 43, wherein the amount of variable delaying is based on the quality of a transmission path between a transmitter and the receiver.

45. The method of claim 43, wherein the amount of variable delaying is based on noise affecting the transmission of data between a DTE and the receiver.

46. The method of claim 39, wherein the amount of variable delaying is three bauds.

47. The method of claim 39, wherein the step of performing logic calculations is accomplished using a plurality of binary exclusive-OR gates and a plurality of binary AND gates.

48. The method of claim 39, wherein the method is accomplished with firmware.

49. The method of claim 39, wherein the method is implemented using software that is executed with a processor.

50. A computer readable medium for encoding information, comprising:

(a) logic for receiving a data input, the data input being a portion of a data symbol;

(b) logic for variably delaying a plurality of prior data inputs, the plurality of prior data inputs being a portion of each of a plurality of prior data symbols;

(c) logic for storing the variably delayed plurality of prior data inputs;

(d) logic for performing logic calculations;

(e) logic for receiving a coefficient input; and

(f) logic for producing an output, the output being based on the operation of the logic for receiving a data input, the logic for variably delaying a plurality of prior data inputs, the logic for storing the variably delayed plurality of prior data inputs, the logic for performing logic calculations, and the logic for receiving coefficient input.

51. The system of claim 50, wherein the data input is a portion of a PAM symbol.

52. The system of claim 50, wherein the plurality of prior data inputs are each a portion of a PAM symbol.

53. The system of claim 50, wherein a receiver determines the value of the variable delay of the logic for variably delaying a plurality of prior data inputs.

54. The system of claim 50, wherein a receiver dynamically determines the value of the variable delay of the logic for variably delaying a plurality of prior data inputs.

55. The system of claim 54, wherein a value of the variable delay is based on the quality of a transmission path between a transmitter and the receiver.

56. The system of claim 54, wherein a value of the variable delay is based on noise affecting the transmission of data between a DTE and the receiver.

56. The system of claim 50, wherein a value of the variable delay is three bauds.

57. An interleaved generalized convolutional decoder, comprising:

(a) a metric calculator, the metric calculator being capable of receiving an encoded input, the encoded input being a symbol encoded by an interleaved generalized convolutional encoder;

(c) a variable plurality of metric memory elements, the metric calculator configured to produce an output based on metrics associated with the encoded input, the metrics being based on previous states associated with the encoded input, the previous states being stored in the metric memory element associated with the encoded input;

(d) a variable plurality of path memories;

(e) a trellis decoder, the trellis decoder configured to determine a final state and a decoded databit based on the encoded input, the output of the metric calculator, and the path memory associated with the encoded input.

58. The decoder of claim 57, wherein the encoded input is a PAM symbol.

59. The decoder of claim 57, wherein the variable plurality of metric memories is determined by a receiver.

60. The decoder of claim 59, wherein the receiver dynamically determines the variable plurality of metric memories.

61. The decoder of claim 60, wherein the receiver dynamically determines the variable plurality of metric memories based on the quality of a transmission path between a transmitter and the receiver.

62. The decoder of claim 60, wherein the receiver dynamically determines the variable plurality of metric memories based on noise affecting the transmission of data between a DTE and the receiver.

63. The decoder of claim 57, wherein the three metric memories are used.

64. The decoder of claim 57, wherein the variable plurality of metric memories is determined by a receiver.

65. The decoder of claim 57, wherein the decoder is implemented with software that is executed with a processor.

66. The decoder of claim 57, wherein the decoder is implemented with firmware.

67. An interleaved generalized convolutional decoder, comprising:

(a) a subdecoder, capable of receiving an encoded input, the encoded input being a symbol encoded by an interleaved generalized convolutional encoder, the subdecoder including:

(i) a metric calculator;

(ii) a metric memory element, the metric calculator configured to produce an output based on metrics associated with the encoded input, the metrics being based on previous states associated with the encoded input, the previous states being stored in the metric memory element;

(iii) a path memory; and

(iv) a trellis decoder, the trellis decoder configured to determine a final state and a decoded databit based on the encoded input, the output of the metric calculator, and the path memory associated with the encoded input; and

(b) a variable plurality of symbol memories; and

(c) a switching system, the switching system configured to select the memories sequentially based on the level of interleaving associated with the encoded input.

68. The decoder of claim 67, wherein the variable plurality of symbol memories are shift registers.

69. The decoder of claim 67, wherein the encoded input is a PAM symbol.

70. The decoder of claim 67, wherein the variable plurality of symbol memories is determined by a receiver.

71. The decoder of claim 70, wherein the receiver dynamically determines the variable plurality of symbol memories.

72. The decoder of claim 70, wherein the receiver dynamically determines the variable plurality of symbol memories based on the quality of a transmission path between a transmitter and the receiver.

73. The decoder of claim 70, wherein the receiver dynamically determines the variable plurality of symbol memories based on noise affecting the transmission of data between a DTE and the receiver.

74. The decoder of claim 67, wherein three symbol memories are used.

75. The decoder of claim 67, wherein the decoder is implemented with software that is executed with a processor.

76. The system of claim 67, wherein the decoder is implemented with firmware.